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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,059	06/24/2003	Charles N. Perez	BUR920030032US1	1058

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EXAMINER	
DOAN, NGHIA M	
ART UNIT	**PAPER NUMBER**
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/604,059	PEREZ ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amed. 02/09/07 and Sup. Amend. 3/14/07*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20070315*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is response to the Applicant amendment filed on 02/09/2007 and Supplemental amendment filed on 03/14/2007.

2. The claims 1, 5, 13, 17, 25, 29-30, 33, 35-36, 38-39, 42, and 44 remain pending. Claims 1, 13, and 25 have been amended. Claims 2-4, 6-12, 14-16, 18-24, 26-28, 31-32, 34, 37, 40, 41, and 43 have been canceled in the previous office actions.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 5, 13, 17, 25, and 29-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Ker et al. (hereinafter as "Ker"), *Automatic methodology for placing the guard rings into chip layout to prevent latchup in CMOS IC's, IEEE, Vol. 1, September 2001, Pages 113-116.*

5. With respect to claims 1, 13, and 25, Ker discloses a computer storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of displaying a guard ring within (hierarchical) *(the double guard rings are often used to surround the output PMOS and NMOS in I/O cells ... the additional guard rings should be placed between the I/O cells and the Internal circuits.)(Page 113, col. 2, paragraph 3 and figures 3 and 4(b))* an integrated circuit

design having logic devices *("Guard Ring Automation" program to realize the additional guard rings in the layout is proposed to make the layout more automatically and accurately)(The Abstract, page 113)*, said method comprising:

determining positions of said logic devices within *(claim 13, a portion of said hierarchical)* said integrated circuit design *(the location to be added the additional guard rings (figure 5, Page 115, col. 1, paragraph 2; the signal lines such as a, b, c, d, e, and f pass through the region where to be added the guard ring (figure6, page 115, paragraphs 1 and 2); and the double guard rings are often used to surround the output PMOS and NMOS in I/O cells ... the additional guard rings should be placed between the I/O cells and the Internal circuits.)(page 113, col. 2, paragraph 3)*;

incorporating *(forming/adding)* said guard ring into *(claim 13, said portion of said hierarchical)* said integrated circuit design *(automatically place the guard ring in the chip layout to improve latchup immunity of the CMOS IC's (the Abstract); Guard rings are formed by the p+ diffusions in the p-substrate connect to VSS and the n+ diffusions in the n-well connect to VDD. To effectively absorb the trigger current in the well or substrate, the contacts for connection to guard rings should be added as many as possible, (Page 114, Section 2. Guard Rings Automation) and figures 5 and 6 show the guard rings before and after added)*; and

displaying *(claim 13, said portion of)* said logic devices and guard ring symbolically *(figs 3 through fig. 8)* and schematically (circuit) *(figs 3 through fig. 8)* in a single integrated display *(the instance show in Fig. 4(a) and 4(b) are displayed in the master layout views. To simplify the display in the top-level design....)(page 114,*

section 2.1 Instance and Mosaic, figure 4 descriptions), wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol *(figure 4 and its description as page 114-115)* wherein said parameterized symbol comprises parameters (IO guard ring, Additional guard ring, p+ diffusion, n+ diffusion, Power line, signal lines... etc)(figs. 1-6,with the description) wherein said parameters comprise at least one of a type of said guard ring *(n-type and p-type of guard rings)(figure 4 and its description as page 114-115)* and an efficiency of said guard ring *(the program will use instance to get the most area efficiency in the guard ring placement. Thus, the proposed Guard Ring Automation program gets a balance between the speed and the are efficiency to add the additional guard rings for latchup prevention)(type of guard rings such as p-diffusion ring and n-diffusion ring; dimension of guard ring such as D horizontal= the width of guard ring region, D vertical= the height of guard ring region; placement depending on the shape of guard ring such as non-rectangle shape use the instance to add the guard ring and rectangle shape use mosaic to add the guard ring; the electrical connection of guard ring such as p+ diffusions in the p-substrate connect to VSS and the n+ diffusions in the n-well connect to VDD) (pages 114-115 and figures 3-6 and 8).*

6. With respect to claims 30 and 39, Ker discloses all the limitations in set forth claims, further comprising displaying said logic devices and said guard ring graphically in said single display *(pages 114-116 and figures 3-6 and 8).*

7. With respect to claims 5, 17, and 29, Ker discloses all the limitations in set forth claims wherein said displaying of said logic devices displays and said guard ring

graphically comprise illustrating relative position of said logic device and guard ring *(W instance and H instance; D horizontal and D vertical) (figures 4 and 5 and their descriptions; and pages 114-115)*.

8. With respect to claims 33, 35-36, 38, 42, and 44, Ker discloses all the limitations in set forth claims, wherein said displaying of said parameterized symbol comprises displaying said parameters including *(as per claims 33, 35-36, 38, 42, and 44)* a type of circuit *(p-substrate/n-well, I/O circuit and internal circuit)* and *(as per claims 35, 38, and 44)* an efficiency of said guard ring *(the program will use instance to get the most area efficiency in the guard ring placement. Thus, the proposed Guard Ring Automation program gets a balance between the speed and the are efficiency to add the additional guard rings for latchup prevention) (type of guard rings such as p-diffusion ring and n-diffusion ring; dimension of guard ring such as D horizontal= the width of guard ring region, D vertical= the height of guard ring region; placement depending on the shape of guard ring such as non-rectangle shape use the instance to add the guard ring and rectangle shape use mosaic to add the guard ring; the electrical connection of guard ring such as p+ diffusions in the p-substrate connect to VSS and the n+ diffusions in the n-well connect to VDD) (pages 114-115 and figures 3-6 and 8)*.

Examiner Remarks

9. Acknowledgment is made of Applicant's arguments filed on 02/09/2007 and Supplemental Amendment filed on 03/14/2007, which removes the term "simultaneously" from the claimed invention. Hence, the Applicant argument filed on

02/09/2007 will be discarded with respect to the term "simultaneously". Other issues are remained.

10. Applicant's arguments filed 02/09/2007 have been fully considered but they are not persuasive. As the following reason below:

11. Applicant(s) state(s) "nothing within Ker discloses a hierarchical integrated circuit design having a parameterized cell and a guard ring".

Examiner respectfully disagree as the following:

Ker, page 114, section 2.1 Instance and Mosaic, fig. 4(a) is display as single metal layer and fig. 4(b) has multiple metal layers, but forbidden VIA stack. Guard ring are formed by the p+ diffusion in p-substrate connected to VSS and n+ diffusion in n-well connected to VDD. As page 115 and fig. 5(a)-5(d) through fig. 6(a) and fig. 6(b) describe an addition guard ring is added under a specified power line, if the power line VDD and insert diffusion layer is an N+ diffusion with N-well substrate and if the power line VSS and insert diffusion layer is an P+ diffusion with P-well substrate. Moreover, one integrated circuit has at least two (2) basis metal layers or multiple metal layer, such as power (VDD) and ground (VSS) to obtain a hierarchical structure. Hence, Ker discloses a hierarchical integrated circuit design having a parameterized cell and a guard ring.

12. Applicant(s) state(s) "Ker do not illustrate the functional device components schematically; instead, "layout views" showing component "shape" are displayed without schematics".

Examiner respectfully disagree as the following:

13. One of ordinary skill in the art or in the technically that the fig. 4 is layout of circuit design. The layout must be constructed from a schematic (circuit). Moreover, figs. 1-3 show the type of guard ring, where the guarding to be located in the circuit structure and the circuit structure equivalent as circuit (schematic) (fig. 1(a) and fig. 1(b)). Therefore, Ker is including a schematic (circuit design).

14. According to all the evidences above (including citations recited in claim rejection). Ker discloses every limitation of the claim invention. Therefore, the claim rejection is sustained.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. PTO-892.

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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